

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Cancelled)
2. (Cancelled)
3. (currently amended) The method of claim 8, wherein said first plurality of signals data patterns contains and said second plurality of signals are identical data pattern.
4. (Cancelled)
5. (Cancelled)
6. (Cancelled)
7. (currently amended) The method of claim 12, further comprising shifting a data pattern of said first plurality of signals data patterns by at least one bit from said second plurality of signals prior to said repeating to generate said different data pattern of said first plurality of data patterns.
8. (currently amended) A method of operating a memory connected to a bus having a plurality of bit lines, said method comprising:
selecting a first group of bit lines from said bus to carry a first plurality of signals data patterns;
selecting at least one of the remaining bit lines from said bus not within said first group to carry a second plurality of signals data pattern;
transmitting one or more of said first plurality of signals data patterns on said first group of bit lines in said bus;

simultaneously transmitting said second plurality of signals data pattern on said at least one of the remaining bit lines; and

performing [[a]] data write/read operation operations at a data storage location in said memory using said bus while and said one or more of said first plurality of data patterns and said second data pattern signals in said transmitting and simultaneously transmitting are present on respective bit lines in said bus.; and

adjusting a delay based on an accuracy of said data read operations.

9. (currently amended) The method of claim 8, wherein said performing includes:

performing reading of data as part of said data write/read operation operations in conjunction with a strobe signal received from a delay locked loop.

10. (currently amended) The method of claim 9, further comprising:

configuring said delay locked loop to provide a said delay to said strobe signal so as to enable latching of said data during reading thereof such that said strobe signal is centered in the middle of data signals.

11. (Cancelled)

12. (currently amended) The method of claim 4 or 8, further comprising:

transmitting a different data pattern of said first plurality of data patterns; and
repeating said transmitting of said second data pattern, simultaneously transmitting, and
said performing data write/read operations and determining.

13. (Cancelled)

14. (currently amended) A system comprising:

a memory chip including a plurality of storage locations to store data;
a bus having a plurality of bit lines; and
a processor connected to said memory chip via said bus and in communication therewith through said bus, wherein said processor is configured to perform the following:

select a first group of bit lines from said bus to carry a first plurality of data patterns;
select at least one of the remaining bit lines from said bus not within said first group to carry a second plurality of data patterns;
transmit one or more of said first plurality of data patterns on said first group of bit lines,
transmit one or more of said second plurality of data patterns on said at least one of the remaining bit lines; and
perform [[a]] data write/read operation operations at one of said plurality of storage locations using said bus ~~while and said one or more of said first and said second plurality of data patterns and said one or more of said second plurality of data patterns are present on respective bit lines in said bus;~~ ; and
adjust a delay based on an accuracy of said data read operations.

15. (Cancelled)
16. (currently amended) The system of claim 14, wherein said processor includes a delay locked loop circuit configured to provide a delayed strobe signal during reading of data as part of said data write/read operations operation, and wherein said processor is configured to adjust a duration of delay for said delayed strobe signal based on accuracy of said data read during said data write/read operation.
17. (original) The system of claim 14, wherein the number of bit lines in said plurality of bit lines is 2^N , where $N \geq 1$.
18. (currently amended) The system of claim 14, wherein said processor is configured to transmit said one or more of said first plurality of data patterns and said one or more of said second plurality of data patterns simultaneously concurrently.
19. (original) The system of claim 14, wherein said processor includes:
a first linear feedback shift register configured to generate said first plurality of data patterns; and

a second linear feedback shift register configured to generate said second plurality of data patterns.

20. (original) The system of claim 14, wherein said processor further includes a decode circuit having a plurality of output lines, wherein each output line is configured to be connected to one of said plurality of bit lines so as to allow transmission of said first and said second plurality of bit patterns on respective bit lines.

21. (original) The system of claim 14, wherein said processor is further configured to shift said first plurality of data patterns by at least one bit from said second plurality of data patterns.

22. (original) The system of claim 14, wherein said processor is further configured to perform transmission of said first plurality of data patterns and said second plurality of data patterns for each bit line in said plurality of bit lines.

23. (currently amended) A system comprising:

a memory chip including a plurality of storage locations to store data;

a bus having a plurality of bit lines; and

a processor connected to said memory chip via said bus and in communication therewith through said bus, wherein said processor is configured to perform the following:

select a first group of bit lines from said bus to carry a first plurality of data patterns;

select at least one of the remaining bit lines from said bus not within said first group to carry a second plurality of data pattern patterns;

transmit one or more of said first plurality of data patterns on said first group of bit lines;

transmit said second plurality of data pattern patterns on said at least one of the remaining bit; and

perform [[a]] data write/read operation operations at one of said plurality of storage locations using said bus and after each bit in said one or more of said first and said second plurality of data patterns and said second data pattern is transmitted on respective bit lines in said bus; and

adjust a delay applied to a strobe signal based on an accuracy of said data read operations.

24. (new) The system of claim 23, wherein said processor is further configured to store said first plurality of data patterns and said second data pattern.
25. (new) The system of claim 23, wherein said processor is further configured to transmit each data pattern of said first plurality of data patterns concurrently with said second data pattern.
26. (new) The method of claim 8, wherein each data pattern of said first plurality of data patterns is concurrently transmitted with said second data pattern.
27. (new) A method of operating a memory connected to a bus having a plurality of bit lines, said method comprising:
 - selecting a first group of bit lines from said bus to carry a first plurality of data patterns;
 - selecting at least one of the remaining bit lines from said bus not within said first group to carry a second plurality of data patterns;
 - transmitting one or more of said first plurality of data patterns on said first group of bit lines,
 - transmitting one or more of said second plurality of data patterns on said at least one of the remaining bit lines;
 - performing data write/read operations at a data storage location in said memory using said bus and said one or more of said first plurality of data patterns and said one or more of said second plurality of data patterns; and
 - adjusting a delay based on an accuracy of said data read operations.
28. (new) The method of claim 27, wherein said performing includes:
 - performing reading of data as part of said data write/read operations in conjunction with a strobe signal received from a delay locked loop.

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29. (new) The method of claim 28, further comprising:

configuring said delay locked loop to provide said delay to said strobe signal such that said strobe signal is centered in the middle of data signals.

30. (new) The method of claim 27, wherein each of said one or more of said first plurality of data patterns is concurrently transmitted with one of said one or more of said second plurality of data patterns.